Dead-Time Compensation of Inverters Considering Snubber and Parasitic Capacitance

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***Abstract*—In power electronics drive systems, dead time is used to prevent shoot-through over power devices. However, dead time can lead to distortion of ac output voltages and currents. Various compensation methods have been proposed to overcome this drawback. However, most strategies assume the power switches as ideal switches and the transition from ON to OFF or vice versa is infinitely fast. In this paper, effects of inverter snubber and parasitic capacitance to the switching instants are investigated when doing dead-time compensation. A new dead-time compensation method is presented with the capacitance being considered. It is verified that the compensation becomes more accurate and effective for the specific application after the modification. It is also shown that the proposed compensation can make the inverter system stable and robust. This proposed approach is validated by the experimental results.**

***Index Terms*—Dead time, pulse-based dead-time compensator (PBDTC), pulse shift, snubber and parasitic capacitance, voltage-second balance.**

I. Introduction

POWER ratings of pulse-width-modulated (PWM) inverters used for hybrid electrical and electrical vehicles vary from a few kilowatts for electric scooters and motorcycles to a few hundred kilowatts for hybrid electrical and electrical passenger cars. However, the voltage rating of a battery pack is always limited due to the technical challenges, safety, and cost considerations. In particular, for scooter and motorcycle applications, the high-power battery pack with low-voltage (<72 V) outputs a large current of several hundred amperes. In such a situation, the fast change of the current over any stray inductor $L{\cdot}di/dt$ can cause serious stress on the power switching devices. To protect the devices, a large snubber capacitor is often used to suppress the over voltage. As noticed previously, the parallel capacitance, including the snubber capacitor and the device internal parasitic capacitance, is substantial and should be properly modeled and investigated to correctly assess the inverter and system performance.

In PWM inverters, all the power switching devices have a finite turn-on and turn-off time. This may cause shoot-through over the power devices at the instant of switchover between the two switches in series across the dc link. A time period, inserted between the switching signals to prevent the conduction overlap, is adopted as dead time. For the traction drive inverter with a large current rating, a dead time of a few microseconds ranging from 2 to 8 is required to ensure reliable current switchover.

Because of the large dead time and the parallel capacitance, the inverter often outputs a distorted voltage. The nonlinearity caused by this output voltage is very detrimental to the performance of the inverter and ultimately leads to very large current harmonics as well as torque ripple. To mitigate the negative effect of dead time, various compensation strategies have been proposed [1]–[19]. Two major types of compensation methods are summarized in terms of compensation objects. For the first type, the dead time is modeled as an average voltage loss where the voltage-second is averaged over a PWM cycle. The lost voltage-second due to dead time is then added directly to the reference voltage [1]–[5]. The second type models the dead-time effect as a pulse shift error and compensated in each PWM period [6], [7]. Several online compensation methods are also proposed to accommodate the modeling errors [8]–[11]. Usually, both of the switches in one phase leg conduct current within one PWM period. Papers [12]–[14] propose a modified switching logic to allow only a single switch in each phase to commutate in each PWM period. Paper [14] adapts the similar method as that in [13] using modified hardware to fulfill the task.

However, most previous work assumes that the turn-on and turn-off of power switching devices are infinitely fast and few literature works examine the effects of parallel capacitance to dead-time compensation. The nonlinearity between phase current and dead-time voltage error is tested and compensated based on the offline measurement [16]. In [17], the parasitic capacitor is treated as a linear fictitious resistor only when the phase current is below certain value. In [18], the finite response of the power switch device during turn-on and turn-off intervals is studied and its effect on flux estimation is investigated. In [19], numerous parasitic effects on voltage source inverter are identified and qualified with limited compensation discussion. Paper [20] delivers the similar statement of the effect of parasitic capacitance on dead time. However, the inaccuracy of compensation is not well summarized and compared thoroughly. Moreover, most of the compensations are gauged based on the offline measurement without detailed modeling.

This paper examines the inverter operating details during dead time with the effects of device parallel capacitance considered. In Section II, the dead time, the dead-time voltage error, and conventional pulse-based dead-time compensator (PBDTC) method proposed by Leggate and Kerkman [6] are reviewed and analyzed. In Section III, the dead time and dead-time voltage error

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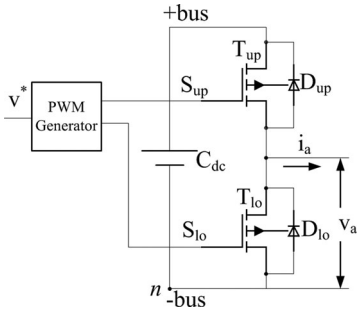

Fig. 1. One phase leg of an inverter.

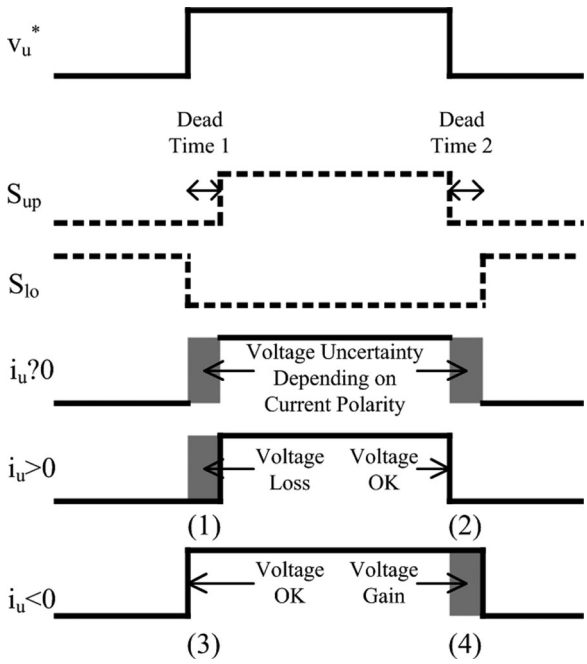

Fig. 2. Gating signals and voltage variation of one phase leg in one PWM cycle.

considering parallel capacitance are modeled and the issue associated with the PBDTC method is investigated in detail. In Section IV, we propose a new dead-time compensation method to generate compensation pulse with reference to different load conditions. In Section V, the experimental results are presented to verify the proposed method.

II. Dead Time and Dead-Time Voltage Error

A. Dead Time and Dead-Time Voltage Error

In order to clearly explain the dead time and dead-time voltage error, one phase leg of the inverter is used as an example, which is shown in Fig. 1. The circuit in discussion consists of two power devices $T_{\rm up}$ and $T_{\rm lo}$, two freewheeling diodes $D_{\rm up}$ and $D_{\rm lo}$, and the dc-bus capacitor $C_{\rm dc}$. A PWM generator sends out PWM signals to gate the power switches. This phase leg u is connected to the motor phase terminal. Its current i_u is defined positive when it flows into the motor.

The gating signals and voltage waveforms in one PWM cycle including the dead time are shown in Fig. 2, where v_u^* is the phase

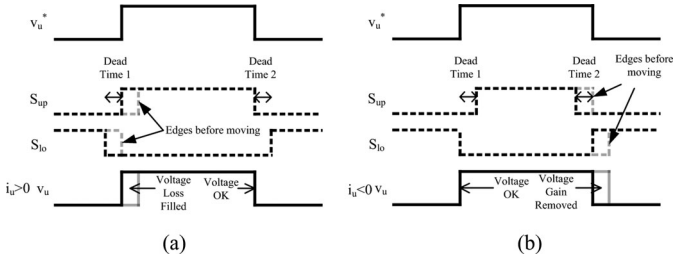

Fig. 3. Voltage error correction with the PBDTC method. (a) Compensation for positive current. (b) Compensation for negative current.

u command voltage for the PWM generator. Two gating signals, $S_{\rm up}$ and $S_{\rm lo}$, are used to control the upper and lower devices in the phase leg with the dead time added. The actual phase voltage waveform v_u appears floating during the dead time. Actually, the phase current i_u conducts through freewheeling diode either $D_{\rm up}$ or $D_{\rm lo}$. For different current polarities and voltage changing edges, four cases can be separately considered to investigate the voltage error due to dead time.

1) i_u is positive at the instant when $T_{\rm lo}$ turns OFF and $T_{\rm up}$ turns ON. The phase current is supposed to switch to $T_{\rm up}$ instantaneously, which pulls up the phase voltage to +bus. However, the dead time forces the current flowing in $D_{\rm lo}$. Voltage loss occurs in this situation.
2) i_u is positive at the instant when $T_{\rm up}$ turns OFF and $T_{\rm lo}$ turns ON. The current is supposed to flow through its lower switch $T_{\rm lo}$ with phase u pulling down to –bus if no dead time is added. The current flows through $D_{\rm lo}$ actually, which presents the same phase voltage as that of the ideal situation. There is no voltage loss or gain in this scenario.
3) i_u is negative at the instant when $T_{\rm lo}$ turns OFF and $T_{\rm up}$ turns ON. The upper diode $D_{\rm up}$ carries the freewheeling current during the dead time till it ends. The correct voltage is applied to the motor terminal.
4) i_u is negative at the instant when $T_{\rm up}$ turns OFF and $T_{\rm lo}$ turns ON. The negative current is blocked by the lower diode $\rm D_{lo}$ and continues to flow in the upper diode $D_{\rm up}$. Voltage gain appears in this case.

B. PBDTC in [6]

Different from those average voltage value-based compensation methods, the PBDTC method proposed in [6] is based on the modification of pulse edges in each PWM cycle directly. Fig. 3 shows the switching signals and anticipated phase voltage waveforms after compensation. The lost voltage block at the rising edge of the phase voltage in Fig. 3(a) is filled up by shifting the pulse edges of both the upper and lower switches ahead at the length of the dead time. In Fig. 3(b), the gained voltage is removed using the same method. Consequently, the command voltage v_u^* and actual voltage v_u becomes identical after the compensation. The PBDTC method requires barely any hardware modification and the minimum software coding, which makes it really efficient. The experiment results in [6] demonstrated that this method can effectively minimize the current harmonics.

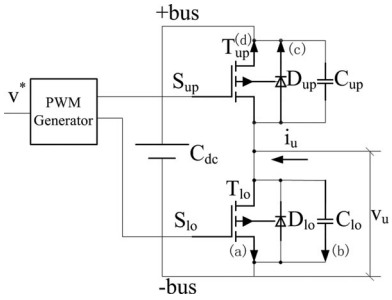

Fig. 4. One phase leg of an inverter with snubber and parasitic capacitance.

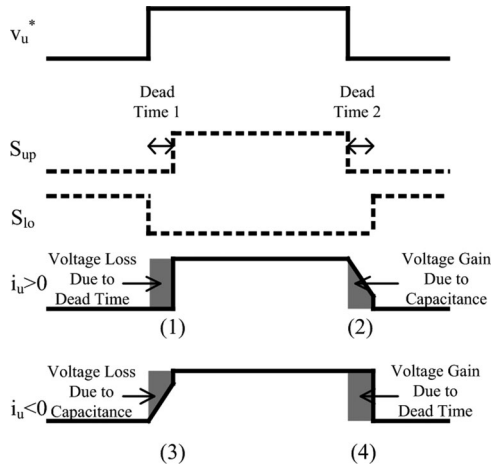

Fig. 5. Gating signals and voltage variation of one phase leg in one PWM cycle with parasitic and snubber capacitance considered.

III. Dead Time Considering Snubber and Parasitic Capacitance

The dead-time compensation aforementioned is based on the assumption that the phase voltage switching edge is ideally sharp. However, the fact is that the turn ON and turn OFF of power switches cannot be infinitely fast and the phase voltage cannot change instantly either. The real voltages in each PWM cycle changes with slopes, especially when an additional snubber capacitor is added. The inverter with parallel drain to source snubber capacitor is modeled in the following section. The associated problems caused by this parallel capacitance to the PBDTC method are investigated. Voltage–second balance principle is applied here in each PWM cycle.

A. Current Switchover Considering Snubber and Parasitic Capacitance

Using the same analysis method as in Section II, the phase voltage variation considering the parallel capacitance is examined here. The original phase leg circuit in Fig. 1 changes to that in Fig. 4 by adding two parallel capacitors. Considering the different phase current signs and switching edges, four possible switching cases are separately described below. Fig. 5 shows the switching signals and phase voltage waveforms.

1) i_u is positive at the instant when $T_{\rm lo}$ turns OFF and $T_{\rm up}$ turns ON. v_u stays low till the end of dead time. At this moment, $C_{\rm up}$ holds the dc-bus voltage and voltage on $C_{\rm lo}$ is zero. After $T_{\rm up}$ changes from OFF to ON, i_u switches from $D_{\rm lo}$ to $T_{\rm up}$. Now, $C_{\rm lo}$ is connected to the dc bus through $T_{\rm up}$. This pumps up the voltage on $C_{\rm lo}$ due to the large charging current. The upper capacitor $C_{\rm up}$ discharges itself through $T_{\rm up}$. In this case, the phase voltage edge is very sharp as shown in Fig. 5.
2) i_u is positive at the instant when $T_{\rm up}$ turns OFF and $T_{\rm lo}$ turns ON. After $T_{\rm up}$ turns OFF, i_u begins to charge the upper capacitor $C_{\rm up}$, which decreases the phase voltage v_u. The voltage's falling slope of v_u is directly proportional to the value of phase current. There can be two different phase voltage profiles in terms of different voltage falling slopes. In Fig. 6(a), the phase voltage is higher than zero at the end of dead time. Then, the voltage is forced to zero when $T_{\rm lo}$ begins to conduct. In Fig. 6(b), the phase voltage reaches zero before the end of dead time. In this scenario, lower diode $D_{\rm lo}$ conducts the phase current till the end of the dead time.
3) i_u is negative at the instant when $T_{\rm lo}$ turns OFF and $T_{\rm up}$ turns ON. This switching process is the reverse process of that in case (2). There are also two possible voltage profiles depending on i_u.
4) i_u is negative at the instant when $T_{\rm up}$ turns OFF and $T_{\rm lo}$ turns ON. Opposite to that in case (1), the phase voltage jumps down instantaneously with a sharp edge.

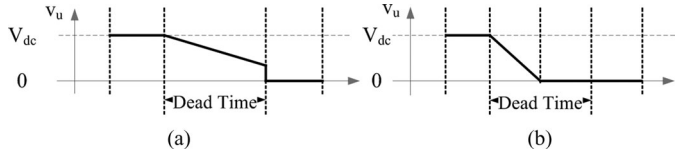

Fig. 6. Different voltage profiles for positive current at voltage falling edge. (a) Phase voltage is higher than zero at the end of dead time. (b) Phase voltage reaches zero before the end of dead time.

In all, the snubber and parasitic capacitance slows down the voltage falling edge when i_u is positive and the voltage rising edge when i_u is negative. This is actually what the snubber capacitor is supposed to do, offering another current path to limit the *di/dt* voltage when the main switch is turning OFF. However, the altered voltage waveform during the dead time as well as its asymmetry to the rising and falling voltage edges makes the modification of the existing dead-time compensation method necessary.

B. Problems Associated With the PBDTC Method

The PBDTC method introduced in Section II can effectively minimize the harmonic components in the phase current. When including the parallel capacitance in the circuit, the PBDTC method no longer behaves correctly. Fig. 7 shows the phase current testing waveforms with and without the PBDTC compensation method under exactly the same modulation index and reference frequency. It is evident that when the PBDTC compensation method is applied, the current peak-to-peak magnitude increases. However, the current waveform is severely distorted with dc offset.

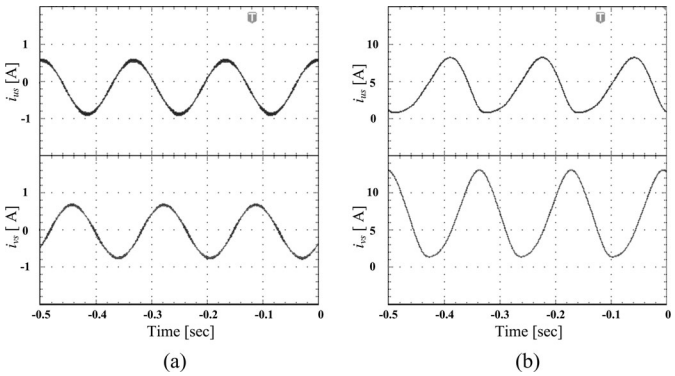

Fig. 7. Inverter phase current output with large snubber capacitor. ($V_{\rm dc}$ = 48 V; Modulation Index = 0.04; Frequency = 120 Hz). (a) Without the PBDTC method. (b) With the PBDTC method.

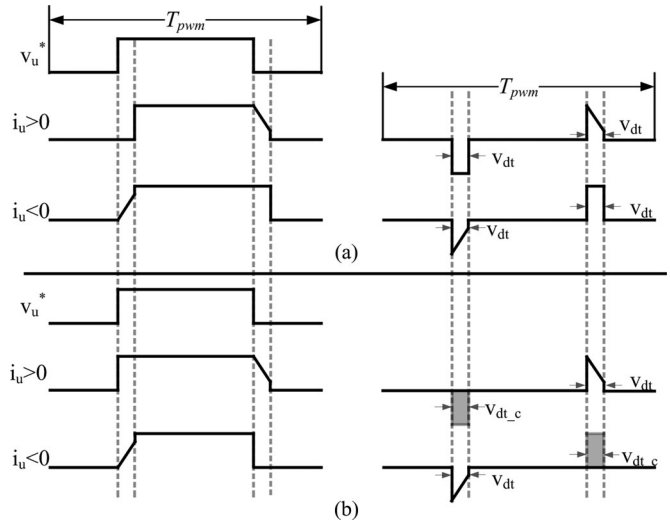

Fig. 8. Phase voltage and its difference between the ideal voltage and the actual voltage. (a) Without compensation. (b) With PBDTC compensation.

Theoretically, for any current distortion, there must be an abnormal voltage component associated with that. The irregular voltage slopes during the dead time mentioned in Section III-A are most likely responsible. Therefore, the dead-time voltage alone in each PWM cycle is analyzed. Fig. 8(a) shows the phase voltage waveform along with the dead-time voltage in one PWM cycle without compensation. Fig. 8(b) shows the one with compensation. In each figure, the topmost curve is the reference voltage v_u^* with the real voltage curves plotted below for both the negative and positive current directions. The right half of the figure shows the voltage difference between the real voltage and the command voltage, which is designated as dead-time voltage. For the positive current in Fig. 8(a), the average dead-time voltage, obtained by averaging the total dead-time voltage over one PWM cycle, is negative. When it comes to the negative current, the average dead-time voltage turns out to be positive. Therefore, the dead-time voltage always holds the opposite sign as that of the phase current. In another word, the dead-time voltage has the tendency to keep the phase current toward zero. When examining the voltage edge slope more carefully, the tendency is aggravated when the magnitude of the current becomes larger.

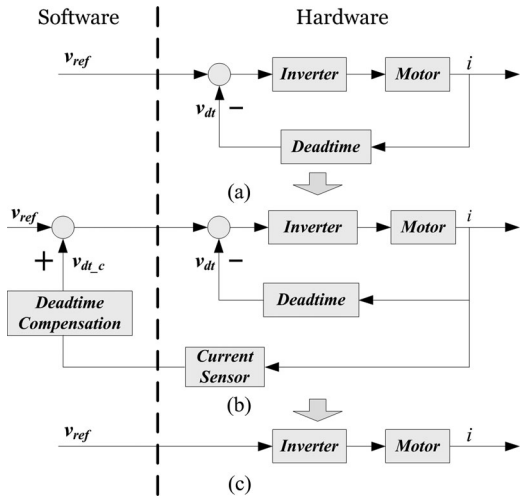

Fig. 9. System diagram of the dead time and dead-time compensation. (a) Controller model without dead-time compensation. (b) Controller model with dead-time compensation. (c) Target model after compensation.

This is mainly because of the larger average dead-time voltage. This can be designated as negative feedback of the dead-time voltage to the phase current. With the PBDTC method applied in Fig. 8(b), either the dead-time voltage notch or the hump is filled up by the compensation voltage for different current polarities. The dead-time voltage now has the same sign as that of the phase current, which reverses the feedback feature of the signal from negative to positive. The system runs into an unhealthy condition which is demonstrated by the abnormal waveforms in Fig. 7(b).

This problem is further analyzed at the system level. The system diagram of the electric drive is plotted in Fig. 9. In Fig. 9(a), a negative path v_{dt} is added to represent the dead-time voltage. As explained before, this feedback voltage stabilizes the system by forcing average phase current toward zero. In Fig. 9(b), the dead-time compensation voltage is introduced as another path from the output current to the reference voltage. Different from the dead-time voltage path, the compensation is coded in the software and shows the opposite sign. The ultimate goal of the dead-time compensation is to use the compensation voltage v_{dt_c} to cancel out the dead-time voltage v_{dt} so that the whole system is linearized as in Fig. 9(c). The PBDTC method models the PWM voltage waveform without considering the parallel capacitor, which leads to the overcompensation of the dead time and moreover the instability issue of the whole system.

IV. Proposed Dead-Time Compensation Method

A. Compensation Principle of the Proposed Method

The analysis above clearly points out the way to the correct solution: Trim the excessive compensation time introduced by the PBDTC method so that the final system is neither overcompensated nor undercompensated. The fully filled notch and hump in Fig. 8(b) are now partially filled by the dead-time compensation voltage v_{dt_c} in Fig. 10. Finally, the dead-time voltages of both the rising and falling voltage edges in one PWM cycle cancel out each other.

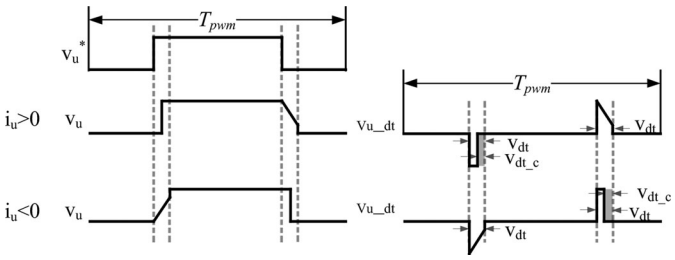

Fig. 10. Phase voltage and its dead-time voltage with the proposed dead-time compensation method.

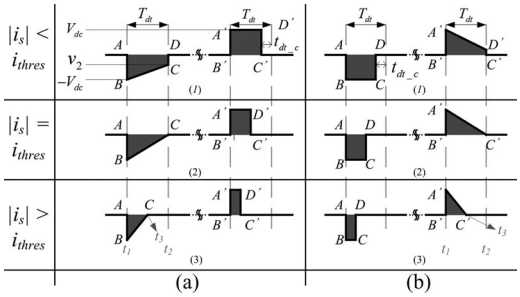

Fig. 11. Phase voltage difference in one PWM period for different phase currents. (a) $i_s < 0$. (b) $i_s > 0$.

B. Derivation of the Compensation Time

Now, the compensation time of the proposed method can be derived based on the aforementioned principle. First, the voltage–current relation on a general capacitor is examined here. The voltage variation on a capacitor with constant current is shown from (1) to (3), where, v_1 is the initial voltage at t_1 and v_2 is the final voltage at t_2. Therefore, for the predetermined dead-time interval, the phase voltage changing speed is proportional to the phase current level and is inversely proportional to the parallel capacitance

$$\frac{dv}{dt} = \frac{i}{C} \tag{1}$$

$$v = \int_{t_1}^{t_2} \frac{i}{C} dt \tag{2}$$

$$v_2 - v_1 = \frac{i}{C}(t_2 - t_1). \tag{3}$$

As mentioned previously, two cases are considered separately for different phase current levels. If the phase current absolute value $|i_s|$ is less than $V_{\rm dc}{\cdot}C/T_{dt}$ ($V_{\rm dc}$—dc-bus voltage; C — parallel capacitance; T_{dt}—dead time), the dead time elapses before the phases voltage reaches $V_{\rm dc}$. Otherwise, the phase voltage hits $V_{\rm dc}$ before the end of dead time. $V_{dc}{\cdot}C/T_{dt}$ is recognized as the threshold current $i_{\rm thres}$. Fig. 11 shows the dead-time voltage in one PWM period for different current magnitude after compensation. The current sign decides the right edge to be compensated and the current value determines the right amount of time to be compensated. Finally, the area *ABCD* is made to be equal to the area $A'B'C'D'$ in Fig. 11. Table I summarizes all the equations based on the voltage–second balance principle for the negative current.

TABLE I
DEAD-TIME COMPENSATION CALCULATION FOR DIFFERENT CASES

	Voltage-Second Balance Principle [$A_{ABCD} = A_{A'B'C'D'}$]	Compensated Time [t_{dt_c}]
$-i_{thres} < i < 0$	$\frac{1}{2}(-V_{dc}+v_2)\times T_{dt} = -(V_{dc}\times(T_{dt}-t_{dt\_c}))$	$-\frac{i}{2CV_{dc}}T_{dt}^2$
$i = -i_{thres}$	$\frac{1}{2}(-V_{dc})T_{dt} = (-V_{dc})(T_{dt}-t_{dt\_c})$	$\frac{1}{2}T_{dt}$
$i < -i_{thres}$	$\frac{1}{2}(-V_{dc})\times(t_3-t_1) = (-V_{dc})(T_{dt}-t_{dt\_c})$	$T_{dt}+\frac{C}{2i}V_{dc}$

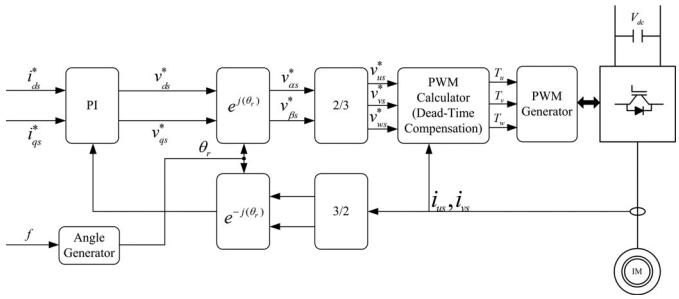

Fig. 12. Experiment control block diagram.

TABLE II
SYSTEM SPECIFICATIONS

Inverter Specifications	Carrier Frequency(PWM)	10[kHz]
	Dead time	6[us]
	DC Bus Voltage	60[V]
Motor Winding Parameters	Stator Resistance	27[mΩ]
	Stator Leakage Inductance	45[uH]
	Rotor Resistance	3.025[mΩ]
	Mutual Inductance	1.2[mH]
Motor Rated Parameters	Rated Power	8[kW]
	Rated line-line RMS Voltage	34[V]
	Rated RMS Current	190[A]
	Rated Stator Frequency	44[Hz]
	Rated Speed	1280[RPM]
Operation Parameters	Synchronous Frequency	6[Hz]
	Reference Current	30[A]
	Rotational Speed	180[rpm]

V. EXPERIMENT INVESTIGATION AND RESULTS

In order to verify the proposed method, an inverter with a controller based on TMS320LF28035 is used to drive an 8-kW induction machine. Fig. 12 shows the control block diagram of this drive system. The compensation algorithm is embedded in the PWM calculator to modify the duty cycles of all the three phases. The specifications of the inverter, the motor, and the operation conditions are listed in Table II. The dead time is set to 6 μs on purpose in order to clearly show the changes after applying the proposed dead-time compensation method.

To highlight the effect of the phase current on the dead-time voltage, the phase voltage and current are tested as shown in Fig. 13. The switching signals of both the upper and lower switches are shown with trace 1 and trace 2. The third trace is the phase voltage and the fourth trace is the phase current.

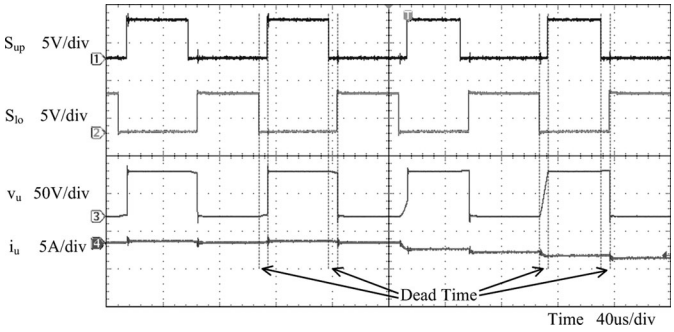

Fig. 13. Gating signals and phase voltage and current waveforms. $S_{\rm up}$: Gating signal for upper switch. $S_{\rm lo}$: Gating signal for lower switch. v_u : Phase voltage waveform. i_u : Phase current waveform.

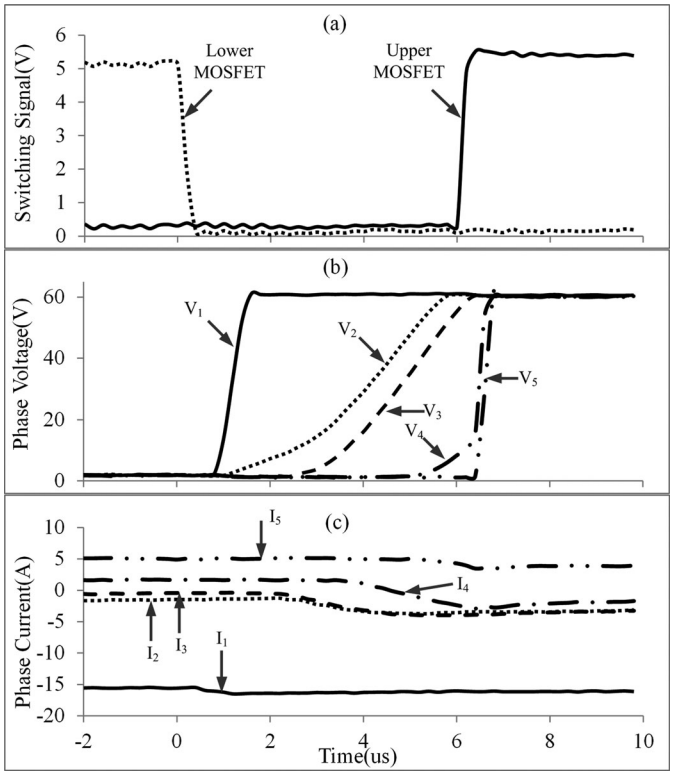

Fig. 14. Rising edge of output voltage for different current level with snubber capacitor during dead time. (a) Gating signals. (b) Phase voltages for different phase current levels. (c) Phase currents.

The phase current stays at zero initially, and the phase voltage maintains its value before and during the dead time and flips over right after the dead time. This is mainly because none of these parallel diodes are conducting during the dead time when the current is near zero. When the phase current slowly becomes negative, the rising edge of the phase voltage v_u changes its rising slope and falling edge still keeps straight, which agrees with the analysis in Fig. 3.

The phenomenon is further investigated by comparing the phase voltage waveforms at different current levels for both the rising and falling edges of the phase voltage in Figs. 14 and 15. For V_1 in Fig. 14(b), its matching current I_1 is around -14 A in Fig. 14(c). After turning the lower switch OFF, this large phase current begins to charge the lower switch parallel capacitance,

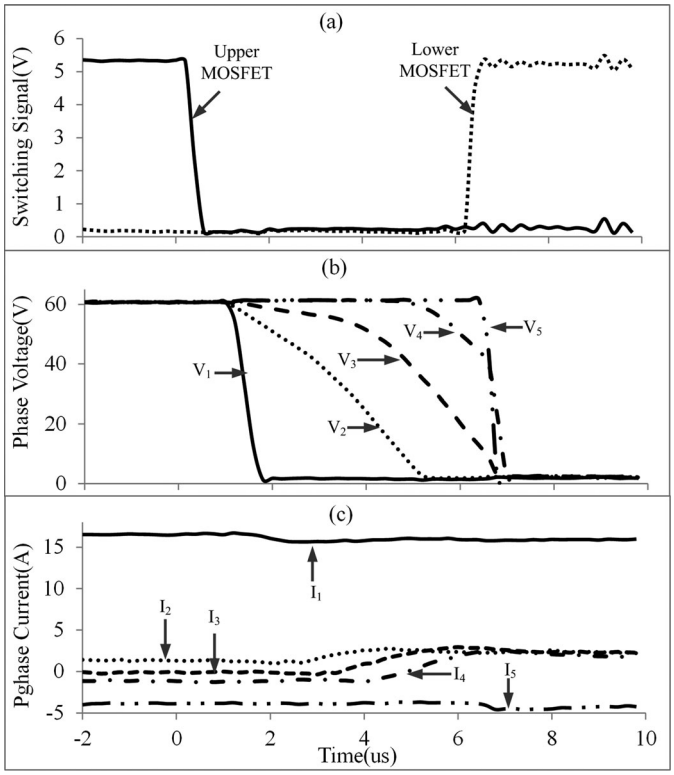

Fig. 15. Falling edge of output voltage for different current level with snubber capacitor during dead time. (a) Gating signals. (b) Phase voltages for different phase current levels. (c) Phase currents.

which makes its phase voltage rising really fast. As for V_2 and V_3 in Fig. 14(b), the magnitude of their matching current I_2 and I_3 in Fig. 14(c) is relatively small, the ramp up speed of the phase voltage becomes slow. The I_4 and I_5 currents deviate further toward its positive direction and the voltage changing behavior above is stressed. Finally, the voltage stays low till the turning ON of the upper switch. For the falling edge of the output voltage, the similar results are obtained in Fig. 15. Therefore, the correlation between the current magnitude and phase voltage waveform has been proved.

In the real experiment, the machine is operated with constant current reference. The phase output current and the command voltage are shown in Figs. 16–19 for both the cases with and without the proposed dead-time compensation. The improvements can be demonstrated in three aspects.

A. Phase Current Distortion Improved

Figs. 16 and 17 show the phase current and its spectrum without and with the proposed dead-time compensation method. The reference current is set to 30 A. In Fig. 16, the current is distorted and the zero current clamping effect is obvious. In Fig. 17, the current maintains sinusoidal and *xy* plot exhibits round shape. The frequency-domain analysis shows the same story. The 5th, 7th, and 11th current harmonics in Fig. 16(c) are larger than that in Fig. 17(c).

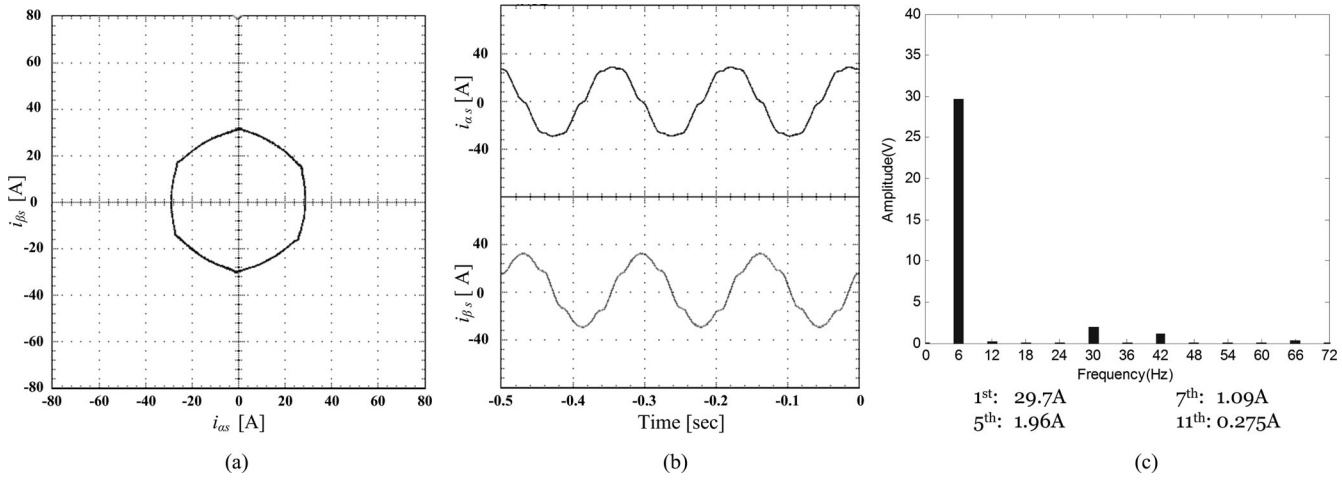

Fig. 16. Phase current without compensation. (a) *xy* plot of current. (b) Current waveforms in stationary frame. (c) Frequency spectrum of the phase current.

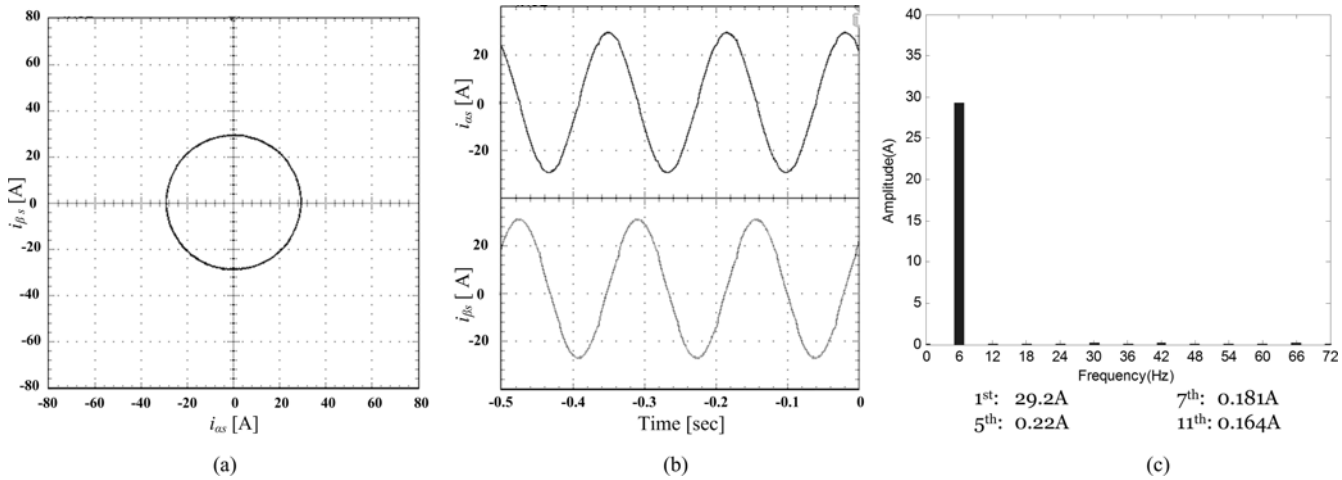

Fig. 17. Phase current with compensation. (a) *xy* plot of current. (b) Current waveforms in stationary frame. (c) Frequency spectrum of the phase current.

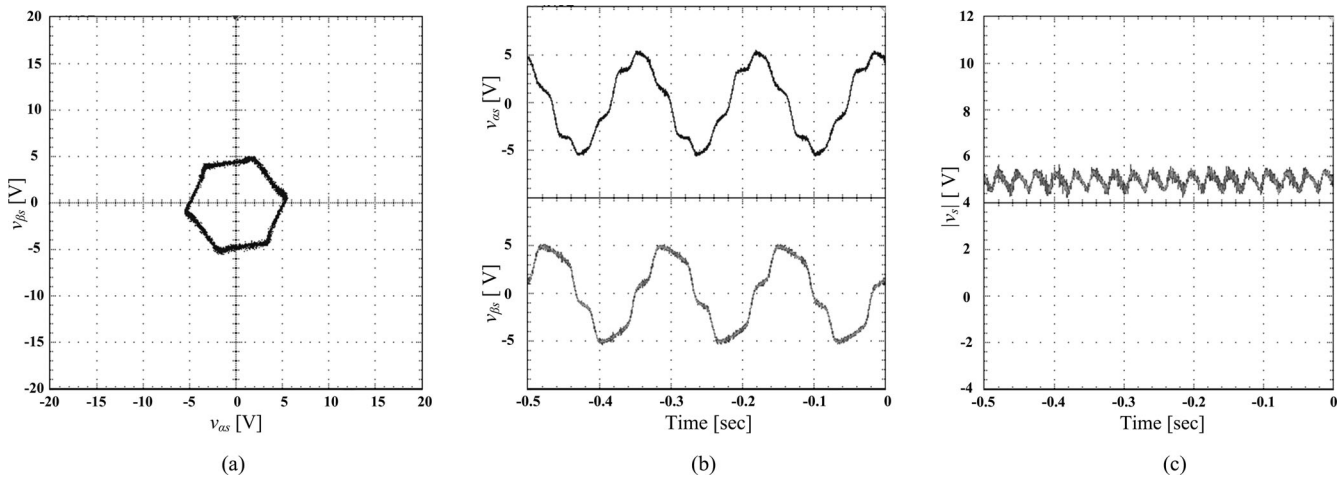

Fig. 18. Phase voltage without compensation. (a) *xy* plot of voltage. (b) Voltage waveforms in stationary frame. (c) Inverter output voltage magnitude.

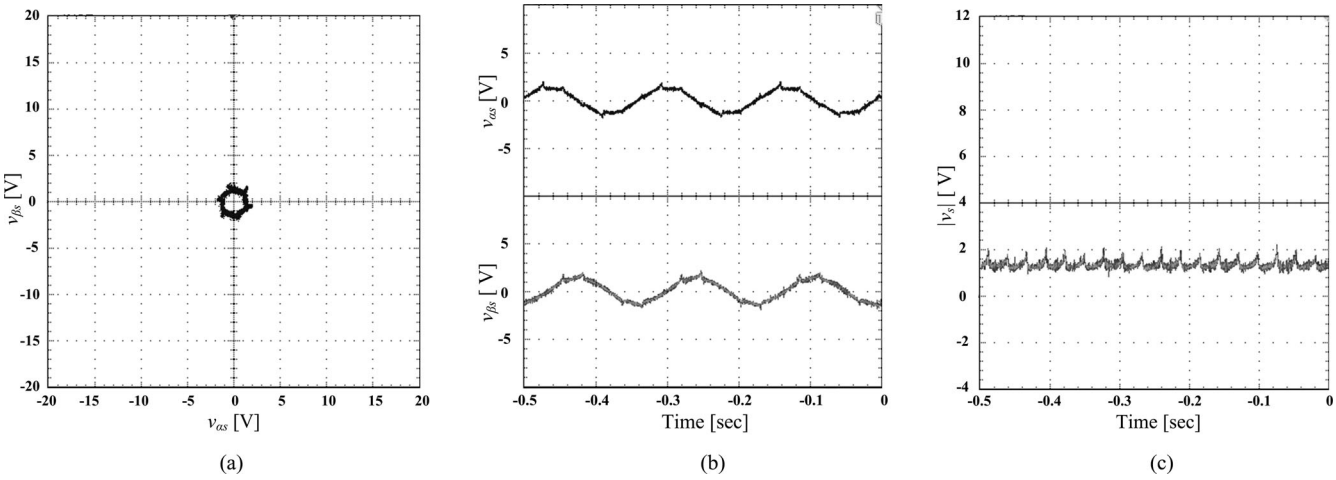

Fig. 19. Phase voltage with compensation. (a) *xy* plot of voltage. (b) Voltage waveforms in stationary frame. (c) Inverter output voltage magnitude.

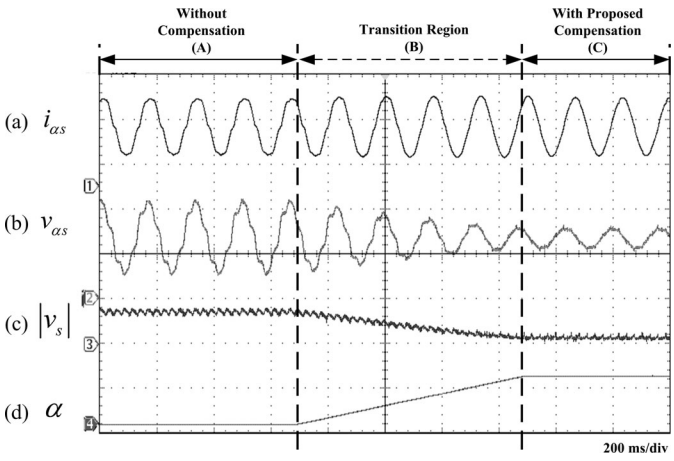

Fig. 20. Experimental result of the transition from no compensation to full compensation. (a) α-axis current. (b) α-axis command voltage. (c) Command voltage amplitude. (d) Weighting function for the proposed compensation.

B. Command Voltage Distortion Improved

The command voltage is obtained from the output of the current controller. Figs. 18 and 19 show this command voltage without and with the proposed dead-time compensation method. In Fig. 18, the voltage is distorted and its *xy* plot shows the regular hexagon shape. The voltage *xy* trajectory shrinks considerably after the compensation in Fig. 19.

C. Command Voltage Amplitude Reduced

With this proposed compensation method, the amplitude of the command phase voltage is greatly reduced for the same reference current. This can be demonstrated by comparing the instantaneous voltage amplitude waveform in Fig. 18(c) before compensation and in Fig. 19(c) after compensation.

Fig. 20 shows the experimental result using the same setup as before. This figure emphasizes the transition process before and after the proposed control. In region A, the compensation is disabled and the system is operating with distorted phase current and phase command voltage. The required phase command voltage amplitude is comparatively high. In region B, a weighting function for the compensation method α is applied from zero to unity, linearly. The system output becomes less noisy with this proposed method applied gradually. In region C, the proposed control is fully activated and the system is operating with minimum voltage requirement.

VI. Conclusion

The dead-time compensation is essential for a drive system to achieve a better steady-state and dynamic performance and also for further algorithm development based on more accurate command voltage. In this paper, a new dead-time compensation method is proposed considering inverter snubber and parasitic capacitance. The following points are covered in this paper:

1) the dead time, the dead-time error voltage as well as the conventional PBDTC method is reviewed;
2) the dead time and dead-time error voltage changes after including snubber capacitors in the circuit;
3) the conventional PBDTC has issue when applying to inverter with large parallel capacitance. This problem is investigated both at the PWM stage and at the system stage;
4) a new modified method is proposed to tackle this problem with minimum software coding;
5) the experiment results verify its effectiveness in reducing current harmonics as well as minimizing the command voltage.

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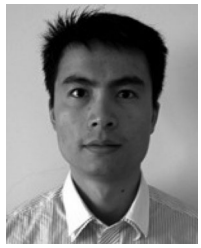

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